DETAILED ACTION

1. The amendment filed 03/30/2010 has been received and considered. Claims 76–79 and 81–83 are presented for examination.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with James Bitetto on 4/19/2010.

4. The application has been amended as follows:

5. Claim 82 line 10, the term "there in" has been replaced with the term --there is--.

Allowable Subject Matter

6. Claims 76–79 and 81–83 are allowed over prior art of record, in light of the arguments filed 09/29/2009, pages 9–13.

7. The following is a statement of reasons for the indication of allowable subject matter:

8. While Levitt et al., U.S. Patent 6,848,088, discloses deriving a model consisting of combinational fanin cones of flip-flops and constraints (see col. 5, lines 49–59; col. 6, lines 5–11; Fig. 2B), and checking correctness on a model; if

the model is proved correct, deeming the circuit design to be correct; otherwise, deeming the verification to be inconclusive (see col. 2, lines 48–57; col. 3, lines 63–67; col. 7, lines 5–13),

Kenneth McMillan, U.S. Patent 6,944,838 discloses design verification using proofs generated from bounded model checkers (see col. 1, 1st paragraph; Fig. 2),

McMillan and Amla, Automatic Abstraction without Counterexamples, (see IDS dated 8/16/08), generates an abstract model for a sequential design of an electronic circuit for verification of a given correctness property, (see pages 5–6),

McMillan et al., U.S. Patent 7,406,405, discloses generating an abstract model for a sequential design of an electronic circuit for verification of a given correctness property (see Fig. 2),

Marques-Silva and Sakallah, GRASP: A Search Algorithm for Propositional Satisfiability (see reference [6] listed in the Application description pg. 3 or PTO-892 Notice of Reference Cited dated 5/15/07) discloses “dummy variables” (see page 518, col. 2, 2nd–5th paragraphs),

Baumgartner, Kuehlmann, and Abraham; Property Checking via Structural Analysis; (see PTO-892 Notice of Reference Cited dated 05/15/2007); discloses abstraction (see pgs. 3, 7, and 8),

and De Moura et al., Pre–Grant publication 2004/0019468, discloses verification based on a lazy combination of a SAT solver with a constraint solver, introducing only the portion of the semantics of constraints that is relevant for constructing a

BMC counterexample (see paragraphs

[0070,0073,0078,0083,0100,0142,0147,0153]).

9. None of these references taken either alone or in combination disclose verification specifically including:

claim 81 "(a) if the given correctness property is proved correct at a depth k, marking only flip-flops and external constraint nodes in the circuit design, based on whether their constraints appear in an unsatisfiable core generated from a proof of unsatisfiability by a satisfiability solver; otherwise, terminating verification, (b) deriving an abstract model consisting of combinational fanin cones of the marked flip-flops and external constraint nodes, (c) checking the given correctness property on the derived abstract model",

claim 82 "(a) if the property is violated at depth k using a satisfiability-based bounded model checking, terminating the verification, (b) if the property is proved correct at depth k using a satisfiability-based bounded model checking, deriving an abstract model A_n from a proof of unsatisfiability generated by the satisfiability solver, (c) increasing the depth of unrolling k in bounded model checking, (d) repeating steps (a-c), constituting an inner loop comprising the bounded model checking iterations, until either there is no change in the size of the derived abstract model as the depth of unrolling k is increased, or some limit kmax on k is reached, (e) repeating steps (a-d) by using bounded model checking on the derived abstract model A_n, to derive a new abstract model A_{n+1}, these steps constituting an outer loop comprising the abstraction iterations, until either there is no change in the size of the derived abstract model or some limit on number of

abstraction iterations is reached",

in combination with and in the same relationship with the remaining elements and features of the claimed invention. Also, there is no motivation to combine none of these references to meet these limitations. It is for these reasons that applicant's invention defines over the prior art of record.

Response to Arguments

10. Applicant's arguments have been fully considered, and they are persuasive.

11. Regarding the Specification objections, the amendment corrected all deficiencies and the objections are withdrawn.

12. Regarding the claim objections, the amendment corrected all deficiencies and the objections are withdrawn.

13. Regarding the rejections under 112, the amendment corrected all deficiencies and the rejections are withdrawn.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan C. Ochoa whose telephone number is (571) 272-2625. The examiner can normally be reached on 7:30AM - 4:00 PM.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571) 272-3753. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/J. C. O./ 4/19/2010

Examiner, Art Unit 2123

/Paul L Rodriguez/

Supervisory Patent Examiner, Art Unit 2123